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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/007,300 ✓
Filing Date November 8, 2001 ✓
Inventor Keiji Jono et al.
Assignee Micron Technology, Inc.
Group Art Unit 2811
Examiner Unknown
Attorney's Docket No. KM1-003
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods of
Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of
Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor,
Trench Isolation Structures Formed in a Semiconductor, Memory Cells and
DRAMS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -See Attached Form PTO-1449


The Examiner's attention is directed to the references which are listed on
the attached Form PTO-1449, copies of which are attached. No admission is
made regarding whether all the submitted references are prior art.

Citation of the referenced art is respectfully requested.

This Supplemental Information Disclosure Statement is being filed before
the mailing date of a first Office Action. Therefore, no fee is believed to be
required. However, in the event that a fee is required for filing this
Supplemental Information Disclosure Statement, please charge the fee specified
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Respectfully submitted,

Dated: 1-28-03

By: 
D. Brent Kenady
Reg. No. 40,045



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PTO/SB/21 (6-98)
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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/007,300
	Filing Date	November 8, 2001
	First Named Inventor	Keiji Jono et al.
	Group Art Unit	2811
	Examiner Name	Unknown
Total Number of Pages in This Submission		Attorney Docket Number KM1-003

ENCLOSURES (check all that apply)		
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	D. Brent Kenady; Reg. No. 40,045; Wells St. John P.S.
Signature	<i>D. Brent Kenady</i>
Date	1-28-03

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